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Novel Detector Implementations Achieving 3G LTE Downlink and Uplink Requirements

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MOTIVATION

- Wireless communication systems have experienced tremendous development during the last two decades. The 4th generation (4G) wireless communication systems and networks will encounter several implementation challenges due to ever increasing capacity and flexibility requirements, whereas the energy budget cannot have similar increase.

- In this paper, we summarize our recent programmable and reconfigurable detector implementations both for uplink and downlink.

- Because of the different energy consumption limitations and hardware resources available in a base station (BS) and in a mobile device (MD), the detector implementations differ significantly beginning already from the algorithm design.
  - In the downlink implementation, we apply a programmable transport triggered architecture (TTA) to provide an energy efficient processor design for detection.
  - In the uplink, we apply a high-end field programmable gate array (FPGA) to implement a K-best list sphere detector (LSD).

ERROR RATE PERFORMANCE

- Fig. 1 presents the downlink comparison for the K-best and the SSFE algorithms. The K-best algorithm outperforms the SSFE algorithm, but requires a sorting operation, which is an expensive operation. Thus, less complex SSFE algorithm is chosen for the downlink implementation.

- Fig. 2 presents the uplink comparison. It can be seen that the 2-stage receiver with a time domain sphere detector using the K-best algorithm outperforms the traditional MMSE equalizer with soft demodulation. The K-best algorithm with list size 8 is chosen for the uplink implementation, because it has lower complexity but the performance is still close to the K-best algorithm with list size 16.

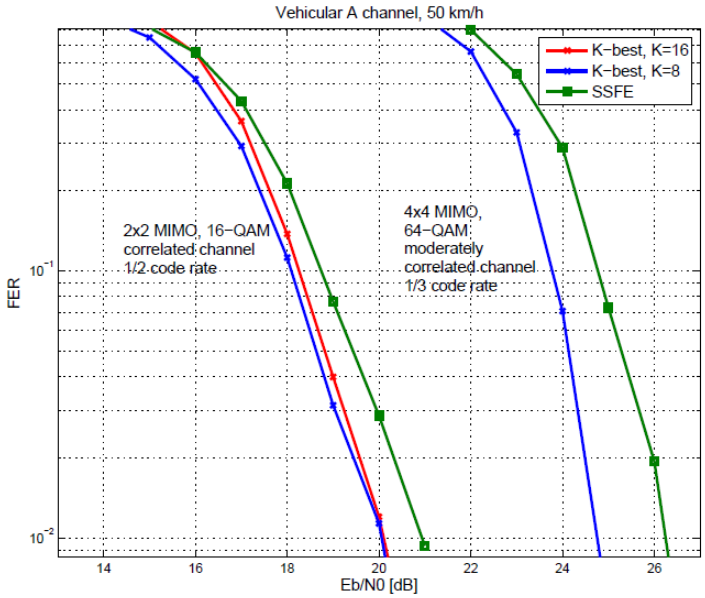

Fig. 1. Detection performance comparison in a vehicular A channel for 2×2 and 4×4 antenna setups in the downlink.

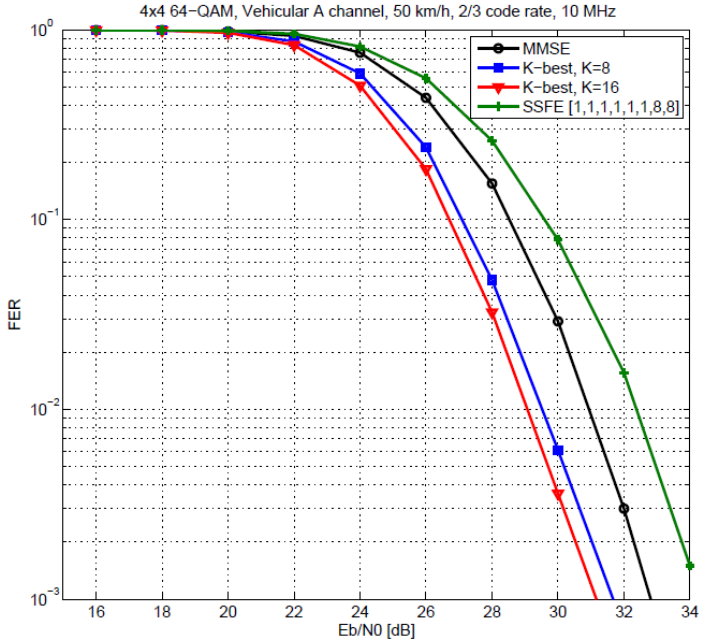

Fig. 2. Detection performance comparison in a correlated vehicular A channel for a 4×4 antenna setup in the uplink.

DOWNLINK IMPLEMENTATION ON TTA

- The downlink implementation is based on the programmable transport triggered architecture (TTA)
- TTA is an architecture template, in which the function units are triggered by data transports
- It is an ideal architecture template to compare different arithmetic implementations due to its low control overhead that is approximately on par with a finite state machine controlled hardware accelerator.
- Block diagram of the TTA accelerator is shown in Fig. 3.

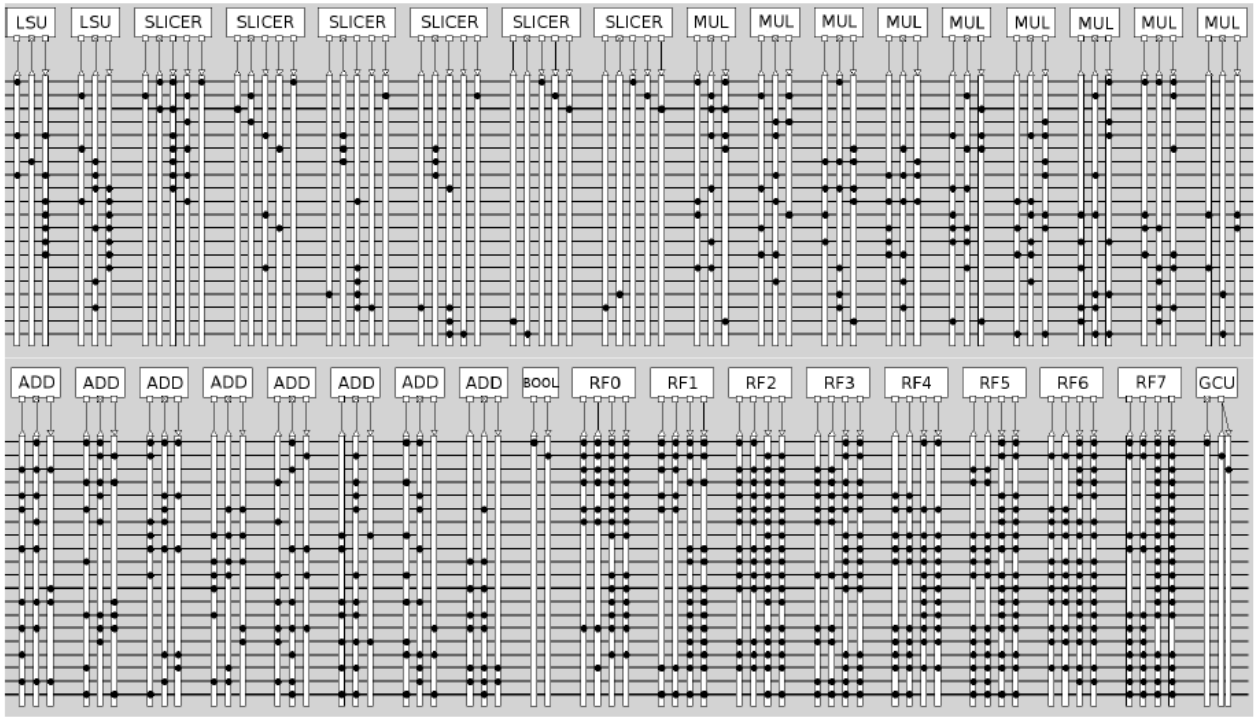

Fig. 3. Block diagram of the TTA accelerator.

DOWNLINK IMPLEMENTATION ON TTA

THE NUMBER OF OPERATIONS DURING THE SSFE ALGORITHM EXECUTION

Operation	# of OPS in 2×2 system	# of OPS in 4×4 system
ADD	54	208
SUB	54	100
MUL	124	313
SLICER	22	47
RF reads	122	367
RF writes	85	135
memory reads	-	21
memory writes	-	27

PROCESSOR POWER AND ENERGY DISSIPATIONS

Processor 4×4 antenna system	16-bit FX (277 MHz)
Total dynamic P (mW)	64.00
Cell internal P (mW)	32.70
Net switching P (mW)	31.20
Total energy (nJ)	22.81
Energy (nJ/bit)	0.95

UPLINK IMPLEMENTATION ON FPGA

- The uplink design is implemented using Xilinx Vivado HLS tool. The tool is used for converting the C code to the register-transfer language (RTL).
- The HLS tool gives a new abstraction level and hides some of the design complexity.
- Xilinx ISE/EDK tools are used for synthesis and place & route.
- The implementation tool flow can be seen in Fig. 4.

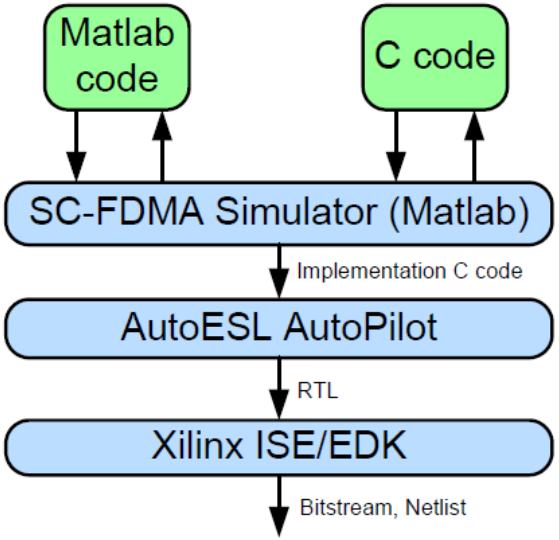

Fig. 4. Tool flow

UPLINK IMPLEMENTATION ON FPGA

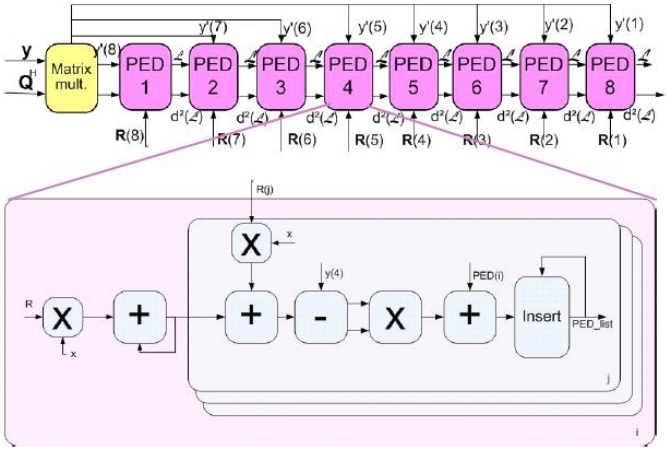

Fig. 5. Block diagram of the Architecture I.

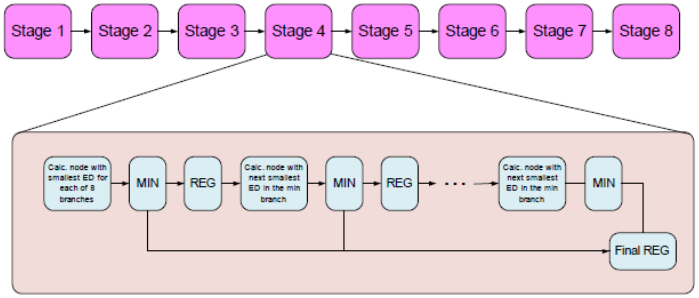

Fig. 6. Block diagram of the Architecture II.

K-BEST ($K = 8$) AREA RESULTS

	Four $II = 64$ blocks	One $II = 16$ block
LUT	34476	69383
FF	50044	97676
DSP48	216	228
BRAM	28	287
Max frequency (MHz)	247	231
Detection rate (Mbps)	372	347

Thank you