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Design of a transport triggered architecture processor for flexible iterative turbo decoder

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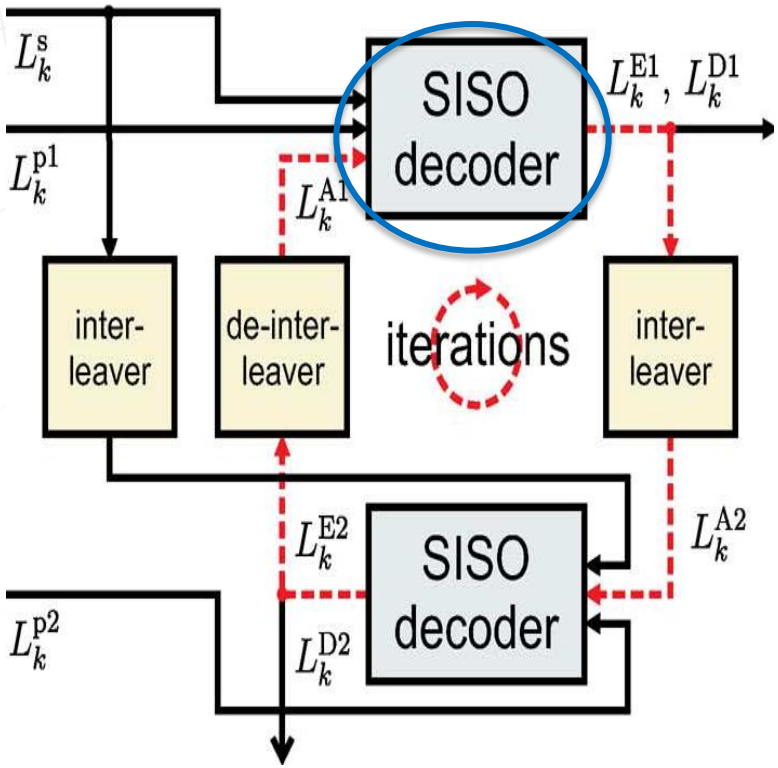
Motivation

- Turbo Coding scheme has been adopted for 3GPP Long Term Evolution (LTE) and IEEE 802.16 e WiMax standards.
- Turbo decoder is one of the most computation intensive part in a 4G wireless receiver.
- ASIC implementations of turbo decoders does not provide flexibility to support multistandard solutions.
- Programmable SIMD/VLIW implementations of turbo decoders offer flexibility but provides lower throughput than ASIC solutions.
- A turbo decoder using transport triggered architecture (TTA) is the next choice for programmable implementations to provide higher throughputs. TTA is a good processor template for application-specific instruction-set processors (ASIP) as it can be easily customized.

The Turbo Decoder



Consists of SISO decoders and interleavers.

The SISO decoding algorithm is the suboptimal forms of radix-2 maximum *a posteriori* (MAP).

Quadratic polynomial permutation (QPP) interleaver and de-interleavers has been used.

Suboptimal MAP Algorithm

The decoding algorithm we are using to implement the SISO decoder is the suboptimal form **Maximum *a posteriori* (MAP)** algorithm.

The optimal MAP algorithm is much more complex than traditional viterbi decoder.

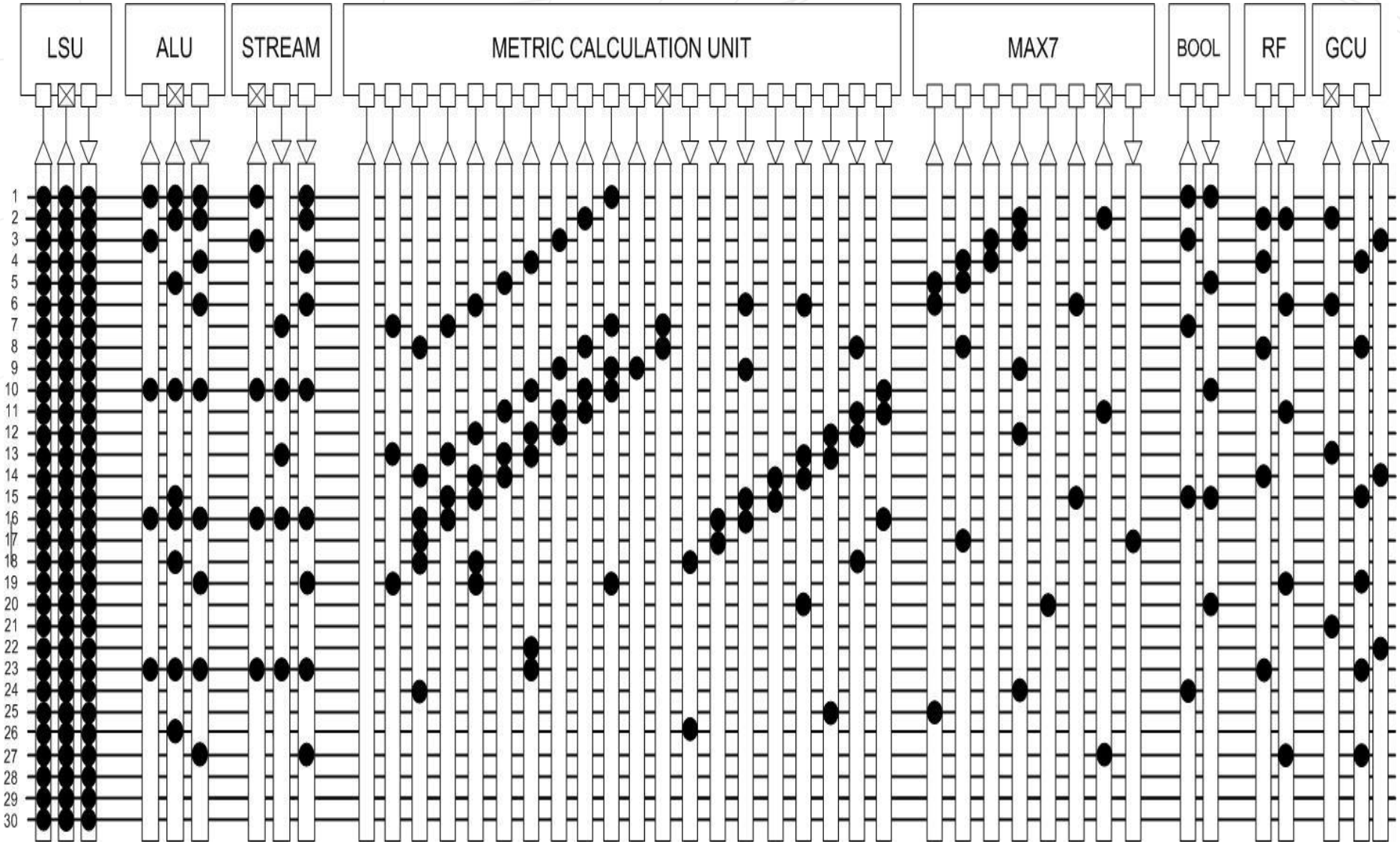
It has a lot of multiplication and exponential operation.

The suboptimal forms of MAP transfers these equations into log arithmetic domain and make the algorithm simpler.

Four suboptimal forms of MAP has been selected for this thesis work:

1. max-log-MAP algorithm.
2. Linear-log-MAP algorithm.
3. Constant-log-MAP algorithm.
4. An approximation of log-MAP algorithm.

Part of the designed processor



The designed processor

The designed processor has the following number of functional units, register files and buses:

1. Five load store unit
2. One arithmetic logic unit
3. Twenty adders
4. One BRANCH SFU
5. One MAX7 SFU
6. One global control unit
7. Thirty buses
8. Nine STREAM SFU
9. Eleven Register Files etc.

The BRANCH metric unit can be used for other algorithms, for instance soft-output viterbi algorithm (SOVA).

Performance Comparison

Modes	Algorithm	Throughput
1	max-log-MAP	31.21 Mbps
2	linear-log-MAP	23.75 Mbps
3	constant-log-MAP	13.32 Mbps
4	log-MAP	2.94 Mbps

Architecture	Throughput	Algorithm
Motorola	243 Kbps	Max- log-MAP
Intel Pentium	366 Kbps	Max-log-MAP
TMS320C6201 DSP	2 Mbps	Max-log-MAP
VLIW ASIP	5 Mbps	Max-log-MAP
TTA proc. for UMTS	14.1 Mbps	Max-log-MAP
Proposed TTA Processor for 3GPP LTE	31.21 Mbps	Max-log-MAP
TTA proc. for 3GPP turbo like code	98 Mbps	Max-log-MAP

Thank you